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Introduction to Hardware

Memory

Agenda

- External memory in IoT product
- Types of semiconductor memory
- Comparison between memories
- Specification

Types of Memory

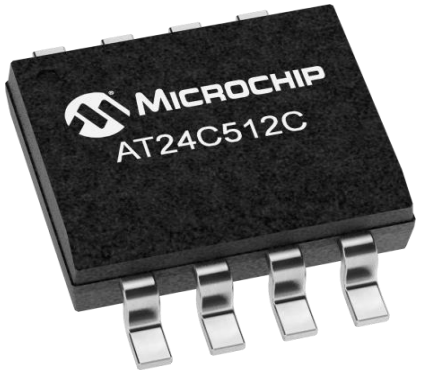
- Volatile
  - RAM
  - Cache
- Non volatile
  - Multi Time Programmable (MTP) and One Time Programmable (OTP)
    - EEPROM (Electrically Erasable Programmable ROM)
    - Flash
      - NAND
      - NOR
    - FRAM (Ferroelectric RAM)

Memory Comparison

	FRAM	Flash	EEPROM
Non-volatile	Yes	Yes	Yes
Write endurance	10^{15}	~ 500,000	~ 1000,000
Write speed	10 ms	30µs (NAND flash) ,120ns (NOR Flash)	2 s
Average active power (µA/MHz)	80	260	10 mA

Source : https://www.digikey.in/en/articles/the-fundamentals-of-embedded-memory

EEPROM



Features

- Low-voltage and Standard-voltage Operation
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 3.6V)
- Internally Organized 65,536 x 8
- Two-wire Serial Interface
- Schmitt Triggers, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1 MHz (5V), 400 kHz (2.7V) and 100 kHz (1.8V) Compatibility
- Write Protect Pin for Hardware and Software Data Protection
- 128-byte Page Write Mode (Partial Page Writes Allowed)
- Self-timed Write Cycle (5 ms Max)
- High Reliability
  - Endurance: 100,000 Write Cycles
  - Data Retention: 40 Years
- Automotive Devices Available
- 8-lead PDIP, 8-lead EIAJ SOIC, 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead LAP, 8-lead SAP and 8-ball dBGA2 Packages
- Die Sales: Wafer Form, Waffle Pack and Bumped Die

Memory Organization **AT24C512, 512K SERIAL EEPROM:** The 512K is internally organized as 512 pages of 128-bytes each. Random word addressing requires a 16-bit data word address.

Source: AT24C512C Microchip Datasheet

NOR Flash

Source :Winbond 25Q128 Datasheet

The W25Q128JV (128M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 1μA for power-down. All devices are offered in space-saving packages.

The W25Q128JV array is organized into 65,536 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q128JV has 4,096 erasable sectors and 256 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See Figure 2.)

The W25Q128JV supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 and I/O3. SPI clock frequencies of W25Q128JV of up to 133MHz are supported allowing equivalent clock rates of 266MHz (133MHz x 2) for Dual I/O and 532MHz (133MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories.

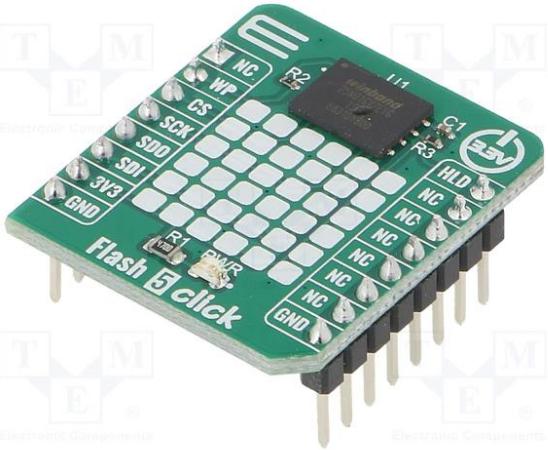
Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP, and a 64-bit Unique Serial Number and three 256-bytes Security Registers.

2. FEATURES

- **New Family of SpiFlash Memories**
  - W25Q128JV: 128M-bit / 16M-byte
  - Standard SPI: CLK, /CS, DI, DO
  - Dual SPI: CLK, /CS, IO_0, IO_1
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Software & Hardware Reset[1]
- **Highest Performance Serial Flash**
  - 133MHz Single, Dual/Quad SPI clocks
  - 266/532MHz equivalent Dual/Quad SPI
  - 66MB/S continuous data transfer rate
  - Min. 100K Program-Erase cycles per sector
  - More than 20-year data retention
- **Efficient "Continuous Read"**
  - Continuous Read with 8/16/32/64-Byte Wrap
  - As few as 8 clocks to address memory
  - Allows true XIP (execute in place) operation
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - <1μA Power-down (typ.)
  - -40°C to +85°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4K/32K/64K-Byte)
  - Program 1 to 256 byte per programmable page
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down
  - Special OTP protection
  - Top/Bottom, Complement array protection
  - Individual Block/Sector array protection
  - 64-Bit Unique ID for each device
  - Discoverable Parameters (SFDP) Register
  - 3X256-Bytes Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
  - 8-pin SOIC 208-mil
  - 16-pin SOIC 300-mil (additional /RESET pin)
  - 8-pad WSON 6x5-mm / 8x6-mm
  - 24-ball TFBGA 8x6-mm (6x4/5x5 ball array)
  - Contact Winbond for KGD and other options

Note: 1. Hardware /RESET pin is only available on TFBGA or SOIC16 packages

NAND Flash



Source : Winbond W25N01GV – Flash5 Mikroelectronica

The W25N01GV (1G-bit) Serial SLC NAND Flash Memory provides a storage solution for systems with limited space, pins and power. The W25N SpiFlash family incorporates the popular SPI interface and the traditional large NAND non-volatile memory space. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 25mA active and 10µA for standby. All W25N SpiFlash family devices are offered in space-saving packages which were impossible to use in the past for the typical NAND flash memory.

The W25N01GV 1G-bit memory array is organized into 65,536 programmable pages of 2,048-bytes each. The entire page can be programmed at one time using the data from the 2,048-Byte internal buffer. Pages can be erased in groups of 64 (128KB block erase). The W25N01GV has 1,024 erasable blocks.

The W25N01GV supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions.

The W25N01GV provides a new Continuous Read Mode that allows for efficient access to the entire memory array with a single Read command. This feature is ideal for code shadowing applications.

A Hold pin, Write Protect pin and programmable write protection, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID, Unique ID page, Parameter page and ten 2,048-Byte OTP pages. To provide better NAND flash memory manageability, user configurable internal ECC, bad block management are also available in W25N01GV.

2. FEATURES

- **New W25N Family of SpiFlash Memories**
  - W25N01GV: 1G-bit / 128M-byte
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Compatible SPI serial flash commands
- **Highest Performance Serial NAND Flash**
  - 104MHz Standard/Dual/Quad SPI clocks
  - 208/416MHz equivalent Dual/Quad SPI
  - 50MB/S continuous data transfer rate
  - Fast Program/Erase performance
  - 100,000 erase/program cycles(4)
  - 10-year data retention
- **Efficient "Continuous Read Mode"(1)**
  - Alternative method to the Buffer Read Mode
  - No need to issue "Page Data Read" between Read commands
  - Allows direct read access to the entire array
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 25mA active, 10µA standby current
  - -40°C to +85/105°C operating range
- **Flexible Architecture with 128KB blocks**
  - Uniform 128K-Byte Block Erase
  - Flexible page data load methods
- **Advanced Features**
  - On chip 1-Bit ECC for memory array
  - ECC status bits indicate ECC results
  - bad block management and LUT(2) access
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - Unique ID and Parameter Pages(5)
  - Ten 2KB OTP pages(3)
- **Space Efficient Packaging**
  - 8-pad WSON 8x6-mm
  - 16-pin SOIC 300-mil
  - 24-ball TFBGA 8x6-mm
  - Contact Winbond for other package options

Notes:
1. Only the Read command structures are different between the "Continuous Read Mode (BUF=0)" and the "Buffer Read Mode (BUF=1)", all other commands are identical. W25N01GVxxxG/R: Default BUF=1 after power up W25N01GVxxxT: Default BUF=0 after power up
2. LUT stands for Look-Up Table.
3. OTP pages can only be programmed.
4. Endurance specification is based on the on-chip ECC or 1bit/528 byte ECC(Error Correcting Code)
5. Please refer to Section 8.2.26 and 8.2.27 for more detail

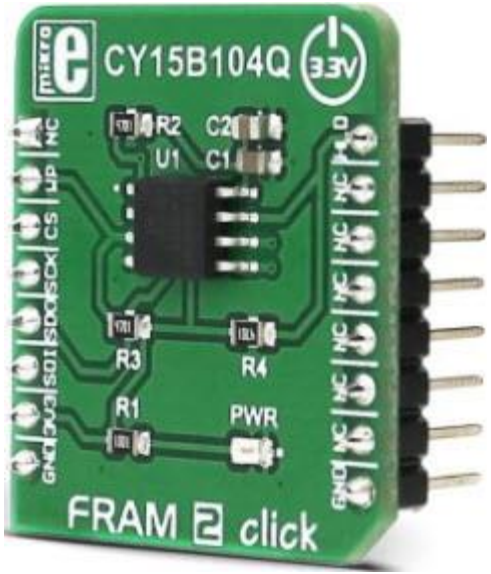
Internal Flash (OTP)

Key Features

- Complies with *Bluetooth V5.0*, ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (J apan)
- Supports up to 8 Bluetooth LE connections
- Fast cold boot in less than 50 ms
- Processing power
  - 16 MHz 32 bit ARM Cortex-M0 with SWD interface
  - Dedicated Link Layer Processor
  - AES-128 bit encryption Processor
- Memories
  - 64 kB One-Time-Programmable (OTP) memory
  - 96 kB Data/Retention SRAM
  - 128 kB ROM
- Power management
  - Integrated Buck/Boost DCDC converter
  - P0, P1 and P2 ports with 3.3 V tolerance
  - Easy decoupling of only 4 supply pins
  - Supports coin (typ. 3.0 V) and alkaline (typ. 1.5 V) battery cells
  - 1.8 V cold boot support
  - 10-bit ADC for battery voltage measurement
- Digital controlled oscillators
  - 16 MHz crystal (±20 ppm max) and RC oscillator
  - 32 kHz crystal (±50 ppm, ±500 ppm max) and RCX oscillator
- Flexible Reset Circuitry
  - System & Power On Reset in a single pin
- General purpose, Capture and Sleep timers
- Digital interfaces
  - Gen. purpose I/Os: 14 (WLCSP34), 25 (QFN40), 32 (QFN48)
  - 2 x UARTs with hardware flow control up to 1 Mbps
  - SPI+™ interface
  - I2C bus at 100 kHz, 400 kHz
  - 3-axes capable Quadrature Decoder
- Analog interfaces
  - 4-channel 10-bit ADC
- Radio transceiver
  - Fully integrated 2.4 GHz CMOS transceiver
  - Single wire antenna: no RF matching or RX/TX switching required
  - Supply current at VBAT3V:
    TX: 3.4 mA, RX: 3.7 mA (with ideal DC-DC)
  - 0 dBm transmit output power
  - -20 dBm output power in "Near Field Mode"
  - -93 dBm receiver sensitivity
- Packages:
  - WLCSP 34 pins, 2.40 mm x 2.66 mm
  - QFN 40 pins, 5 mm x 5 mm
  - QFN 48 pins, 6 mm x 6 mm

Source : https://www.dialog-semiconductor.com/sites/default/files/da14585_datasheet_3v3.pdf

FRAM



Features

- 4-Mbit ferroelectric random access memory (F-RAM) logically organized as 512 K × 8
  - High-endurance 100 trillion (10^{14}) read/writes
  - 151-year data retention (See the Data Retention and Endurance table)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- Very fast serial peripheral interface (SPI)
  - Up to 40-MHz frequency
  - Direct hardware replacement for serial flash and EEPROM
  - Supports SPI mode 0 (0, 0) and mode 3 (1, 1)
- Sophisticated write protection scheme
  - Hardware protection using the Write Protect ($\overline{WP}$) pin
  - Software protection using Write Disable instruction
  - Software block protection for 1/4, 1/2, or entire array
- Device ID
  - Manufacturer ID and Product ID
- Low power consumption
  - 300 µA active current at 1 MHz
  - 100 µA (typ) standby current
  - 3 µA (typ) sleep mode current
- Low-voltage operation: V_{DD} = 2.0 V to 3.6 V
- Industrial temperature: –40 °C to +85 °C
- Packages
  - 8-pin small outline integrated circuit (SOIC) package
  - 8-pin thin dual flat no leads (TDFN) package
- Restriction of hazardous substances (RoHS) compliant

Functional Description

The CY15B104Q is a 4-Mbit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 151 years while eliminating the complexities, overhead, and system-level reliability problems caused by serial flash, EEPROM, and other nonvolatile memories.

Unlike serial flash and EEPROM, the CY15B104Q performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte is successfully transferred to the device. The next bus cycle can commence without the need for data polling. In addition, the product offers substantial write endurance compared to other nonvolatile memories. The CY15B104Q is capable of supporting 10^{14} read/write cycles, or 100 million times more write cycles than EEPROM.

These capabilities make the CY15B104Q ideal for nonvolatile memory applications, requiring frequent or rapid writes. Examples range from data collection, where the number of write cycles may be critical, to demanding industrial controls where the long write time of serial flash or EEPROM can cause data loss.

The CY15B104Q provides substantial benefits to users of serial EEPROM or flash as a hardware drop-in replacement. The CY15B104Q uses the high-speed SPI bus, which enhances the high-speed write capability of F-RAM technology. The device incorporates a read-only Device ID that allows the host to determine the manufacturer, product density, and product revision. The device specifications are guaranteed over an industrial temperature range of –40 °C to +85 °C.

For a complete list of related documentation, click here.

Source: https://www.arrow.com/en/reference-designs/mikroe-2768-fram-2-click-board-based-on-cy15b104q-4-mbit-512k-x-8-serial-fram/0731e3d68ebb548750fe1d3f1e6b1b4e

Source: CY15B104QCY15B104Q Datasheet Cypress

The End